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Title: HIGH-SPEED MEMORY DEVICE, SOCKET MOUNTING STRUCTURE FOR MOUNTING A HIGH-SPEED MEMORY DEVICE AND MOUNTING METHOD OF MOUNTING HIGH-SPEED MEMORY DEVICE

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Masahiko KASASHIMA

Enclosed are:

[**X**] Specification, Claim(s), and Abstract (26 pages).

[**X**] Formal drawings (3 sheets, Figures 1-5).

[**X**] Declaration and Power of Attorney (2 pages).

[**X**] Assignment of the invention to KABUSHIKI KAISHA TOSHIBA.

[**X**] Assignment Recordation Cover Sheet.

[**X**] Claim for Convention Priority and Priority Document.

[**X**] Information Disclosure Statement.

[**X**] Form PTO-1449 with copies of 1 listed reference(s).

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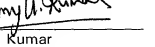
Respectfully submitted,



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TITLE OF THE INVENTION

HIGH-SPEED MEMORY DEVICE, SOCKET MOUNTING STRUCTURE FOR MOUNTING A HIGH-SPEED MEMORY DEVICE AND MOUNTING METHOD OF MOUNTING HIGH-SPEED MEMORY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 11-278225, filed September 30, 1999, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

This invention relates to a high-speed memory device constructed by connecting a plurality of flat high-seed memory modules to one another, each module having input and output side terminals arranged on one side thereof, for dealing with a high-speed signal of plural-bit width, impedance of the high-speed signal being controlled, and the high-speed signal is transmitted from a memory controller to a terminal resistor.

Further, this invention relates to a high-speed memory device constructed by connecting a plurality of flat high-seed memory modules to one another, each module having a metal cover on the surface thereof ,and each module including a connector that has two sets of terminals arranged on one side thereof, for dealing with a high-speed signal of plural-bit width, impedance

of the high-speed signal being controlled.

There is provided a high-speed memory device constructed by connecting a plurality of flat high-seed memory modules to one another, each module having input and output side terminals arranged on one side thereof, for dealing with a high-speed signal of plural-bit width, impedance of the high-speed signal being controlled. The high-speed signal is transmitted from a memory controller to a terminal resistor. As the memory device, for example, there is provided a memory device which is realized by use of the mounting technology of an SO-RIMM (RIMM (Rambus Inline Memory Module) for notebook-sized personal computer proposed by U.S. Rambus Co.).

For the SO-RIMM, a socket (SO-RIMM socket) is used. In the general layout, a memory controller, first SO-RIMM socket, second SO-RIMM socket and terminal resistor are linearly arranged. Further, for a Rambus signal which requires preset impedance precision, a multi-layered circuit board of eight or more layers is used and the impedance matching is maintained by transmitting the Rambus signal through the internal layer of the circuit board.

FIG. 1 shows the outer armor structure of the SO-RIMM. An SO-RIMM 50 has a flat rectangular shape. On one side of the SO-RIMM, connector portions 51a, 51b respectively having input side and output side

terminals for a Rambus signal which is transmitted from a memory controller to a terminal resistor are arranged. Further, a metal cover (heat-spreader also having a function of protection) 52 is disposed on the module surface.

By use of an SO-RIMM socket or sockets, SO-RIMMs are electrically connected to each other, and the SO-RIMM of the above structure is electrically connected to a memory controller, terminal resistor module, clock generator or the like.

If the high-speed memory device is realized by connecting a plurality of SO-RIMMs in a cascade-connection form, a multi-layered circuit board of eight or more layers is used so as to permit the Rambus signal to be transmitted along the internal layer. Therefore, a problem that the cost will be greatly increased occurs. Further, if the Rambus signal is transmitted through the internal layer, it becomes difficult to enhance the impedance precision in comparison with a case wherein the Rambus signal is transmitted along the surface layer. Therefore, there occurs a problem that the manufacturing cost will be raised owing to difficulty in the design and a low manufacturing yield caused by requirement for high precision on the manufacturing process.

BRIEF SUMMARY OF THE INVENTION

An object of this invention is to provide

a high-speed memory device in which high-speed memory modules can be cascade-connected with an inexpensive multi-layered circuit board structure and the impedance for a memory bus signal can be kept constant, a socket mounting structure of the high-speed memory device, and a mounting method for the high-speed memory device.

Another object of this invention is to provide a high-speed memory device for effecting a stable high-speed memory operation with an inexpensive multi-layered circuit board structure by transmitting a high-speed signal of plural-bit width whose impedance is kept constant through a plurality of cascade-connected high-speed memory modules by use of the surface pattern of a multi-layered circuit board, a socket mounting structure of the high-speed memory device, and a mounting method for the high-speed memory device.

Still another object of this invention is to provide a high-speed memory device in which an inexpensive mother board with a less number of layers which is advantageous in cost is used when the high-speed memory device is realized by use of a plurality of SO-RIMMs, a Rambus signal which requires preset impedance precision is wired on the surface layer thereof and the SO-RIMM is stably operated by use of the mother board with an inexpensive layer structure without giving any influence on the Rambus signal

pattern on the mother board even if the SO-RIMM is mounted, a socket mounting structure of the high-speed memory device, and a mounting method for the high-speed memory device.

According to this invention, the above object can be attained by a memory device comprising:

a plurality of storage means for storing information;

means for controlling the storage means;

means, having a resistance, for terminating an electric signal; and

a pattern wiring for electrically connecting the plurality of storage means, the controlling means and the terminating means;

wherein the plurality of storage means, the controlling means and the terminating means are arranged on a board, and the pattern wiring being located in a preset position on the board other than a position in which the storage means is located.

Further, according to this invention, the above object can be attained by a socket mounting structure of a memory device comprising:

a plurality of storage means for storing information;

means for controlling the storage means;

means, having a resistance, for terminating an electric signal; and

a pattern wiring for electrically connecting the plurality of storage means, the controlling means and the terminating means;

wherein the plurality of storage means, the controlling means and the terminating means are mounted on a board, and the pattern wiring being located in a preset position on the board other than a position in which the storage means is located.

Moreover, according to this invention, the above object can be attained by a mounting method of a memory device comprising:

mounting on a board a plurality of storage means for storing information;

mounting on the board a means for controlling the storage means;

mounting on the board a means, having a resistance, for terminating an electric signal; and

mounting on the board a pattern wiring for electrically connecting the plurality of storage means, the controlling means and the terminating means;

wherein the pattern wiring is located in a preset position on the board other than a position in which the storage means is located.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects

and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out hereinafter.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention, and together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. 1 is a view showing the structure of a high-speed memory module (SO-RIMM) according to this invention;

FIG. 2 is a block diagram showing the construction of a memory device according to one embodiment of this invention;

FIG. 3 is a block diagram showing the construction of a memory device according to another embodiment of this invention;

FIG. 4 is a block diagram showing the construction of a memory device according to still another embodiment of this invention; and

FIG. 5 is a block diagram showing a high-speed signal path (Rambus signal path) and the signal direction in the memory device shown in FIG. 4.

DETAILED DESCRIPTION OF THE INVENTION

This invention is to realize a high-speed memory device constructed by connecting a plurality of flat high-speed memory modules (for example, SO-RIMMs), each of which has a metal cover formed on the surface thereof and includes a connector having two sets of terminals arranged on one side thereof, for dealing with a high-speed signal (for example, a Rambus signal) of plural-bit width whose impedance is controlled. That is, high-speed signal lines between the connectors of at least two high-speed memory modules are wired in a portion other than the metal cover surfaces of the high-speed memory modules, and a high-speed signal is transmitted by use of a surface layer pattern of the multi-layered circuit board. As a result, a four-layered or six-layered circuit board (mother board) is used, a line through which the high-speed signal (for example, Rambus signal) with plural-bit width is transmitted is wired on the surface layer, and an influence on the impedance of the Rambus signal wiring can be prevented.

By realizing the high-speed memory device of this invention, a four-layered or six-layered mother board which is advantageous in cost is used, a high-speed memory bus signal line which requires determined preset impedance precision is wired on the surface layer. It becomes possible to stably operate the high-speed

memory module by use of the inexpensive mother board with a less number of layers. It also becomes possible to give little influence on the high-speed memory bus signal pattern on the mother board composed of a less number of layers even if the high-speed memory module is mounted on the mother board.

More specifically, the high-speed memory device is explained in the following embodiment. That is, when a plurality of SO-RIMMs are used to realize the high-speed memory device, a four-layered or six-layered mother board which is advantageous in cost is used without using an eight-layered mother board. At this time, a line through which a Rambus signal is transmitted and which requires preset impedance precision is wired on the surface layer. Further, the line is arranged so as not to give an influence on the Rambus signal pattern on the mother board even when the SO-RIMM is mounted on the mother board. Therefore, the SO-RIMM can be stably operated at high speed with the mother board structure which is advantageous in cost.

There will now be described embodiments of this invention with reference to the accompanying drawings. In this example, the construction and operation of the high-speed memory device are explained by using SO-RIMMs as a plurality of high-speed memory modules constructing the high-speed memory device and using a Rambus signal as a high-speed signal with plural-bit

width whose impedance is controlled.

FIG. 2 is a diagram showing the mounting structure of the high-speed memory device having two SO-RIMMs on the mother board in one embodiment of this invention. In FIG. 2, the mother board is omitted.

In FIG. 2, MEM-CONT 11 denotes a memory controller which is a controller for a Direct Rambus memory. On an SO-RIMM socket 12A, a preceding-stage SO-RIMM 13A is mounted. On an SO-RIMM socket 12B, a succeeding-stage SO-RIMM 13B is mounted. The SO-RIMM 13A is a preceding-stage high-speed memory mounted on the SO-RIMM socket 12A. The SO-RIMM 13B is a succeeding-stage high-speed memory mounted on the SO-RIMM socket 12B. RM 14 denotes a terminal resistor module which is a terminal resistor of the Rambus signal. CLK-Gen 15 denotes a clock generator. A clock signal line 16 is used for a Rambus signal supplied from the terminal side. TI denotes an input side terminal of each of connectors provided on the SO-RIMM 12A and 12B, and TO denotes an output side terminal of each connector.

A pattern wiring 17 is a wiring of the surface layer on the mother board for transferring the Rambus signal from the memory controller (MEM-CONT) 11 to the input side terminal TI of the connector provided on the preceding-stage SO-RIMM 13A mounted on the SO-RIMM socket 12A.

A pattern wiring 18 is a wiring of the surface layer on the mother board for transferring the Rambus signal from the output side terminal TO of the connector provided on the preceding-stage SO-RIMM 13A mounted on the SO-RIMM socket 12A to the input side terminal TI of the connector provided on the succeeding-stage SO-RIMM 13B mounted on the SO-RIMM socket 12B.

A pattern wiring 19 is a wiring of the surface layer on the mother board for connecting the terminal resistor module (RM) 14 to the output side terminal TO of the connector provided on the succeeding-stage SO-RIMM 13B mounted on the SO-RIMM socket 12B.

One-directional arrows shown in the pattern wirings 17, 18, 19 indicate the Rambus signal transferring direction.

In the mounting structure shown in FIG. 2, the SO-RIMM socket 12A on which the preceding-stage SO-RIMM 13A is mounted and the SO-RIMM socket 12B on which the succeeding-stage SO-RIMM 13B is mounted are arranged back to back with a distance of half connector portion shifted from each other.

In other words, the SO-RIMM socket 12A and the SO-RIMM socket 12B are arranged on the mother board so that the output side terminal TO of the connector provided on the preceding-stage SO-RIMM 13A and the input side terminal TI of the connector provided on

the succeeding-stage SO-RIMM 13B will be set to face each other at a close distance.

With the above arrangement and signal wiring thus made, since the Rambus signal does not pass through an area (at least an area of the metal covers of the SO-RIMMs) of the preceding-stage SO-RIMM 13A mounted on the SO-RIMM socket 12A and the succeeding-stage SO-RIMM 13B mounted on the SO-RIMM socket 12B in the pattern wirings 17, 18 and 19, an influence on the impedance (28 ohms±10%) by the metal cover (refer to FIG. 1) of the SO-RIMM can be prevented. Here, the pattern wirings are respectively wired from the memory controller (MEM-CONT) 11 to the SO-RIMM socket 12A, from the SO-RIMM socket 12A to the SO-RIMM socket 12B, and from the SO-RIMM socket 12B to the terminal resistor module (RM) 14.

Therefore, a multi-layered circuit board such as a four-layered or six-layered circuit board which is relatively inexpensive can be used as a mother board and the cost of the whole device can be lowered.

Further, according to the mounting structure of the above embodiment, the pattern wirings 17, 18 and 19 for the Rambus signal are provided on the surface layer of the mother board. Therefore, in comparison with a case wherein the Rambus signal line is wired in the internal layer, it becomes easier to attain preset impedance precision. Further, in comparison with

the conventional mounting structure, the whole wiring length can be reduced by arranging the SO-RIMM sockets 12A, 12B back to back as described above. Therefore, since the size of an area in which the Rambus signal requiring determined impedance (28 ohms±10%) precision is transmitted can be reduced, the pattern design can be more easily made and the stable operation can be expected.

FIG. 3 is a diagram showing the mounting structure in another embodiment of this invention, and in this case, the mother board is also omitted. Portions which are the same as those of FIG. 2 are denoted by the same reference numerals and the explanation therefor is omitted.

In this embodiment, a SO-RIMM socket 12A and SO-RIMM socket 12B are arranged back to back. A memory controller (MEM-CONT) 11 and terminal resistor module (RM) 14 are arranged between the sockets.

Also, in the embodiment shown in FIG. 3, the Rambus signal does not pass through an area (at least an area of the metal covers of the SO-RIMMs) of a preceding-stage SO-RIMM 13A mounted on the SO-RIMM socket 12A and a succeeding-stage SO-RIMM 13B mounted on the SO-RIMM socket 12B in pattern wirings 17, 18 and 19 which are respectively wired from the memory controller (MEM-CONT) 11 to the SO-RIMM socket 12A, from the SO-RIMM socket 12A to the SO-RIMM socket 12B,

and from the SO-RIMM socket 12B to the terminal resistor module (RM) 14. Therefore, an influence on the impedance (28 ohms±10%) by the metal cover (refer to FIG. 1) of the SO-RIMM can be prevented.

Therefore, a multi-layered circuit board such as a four-layered or six-layered circuit board which is relatively inexpensive can be used as a mother board and the cost of the whole device is lowered.

Further, according to the mounting structure of the above embodiment, the pattern wirings 17, 18 and 19 for transmitting the Rambus signal are provided on the surface layer of the mother board. Therefore, in comparison with a case wherein the Rambus signal line is wired in the internal layer, it becomes easier to attain preset impedance precision. Further, the pattern design can be made more easily and the stable operation can be expected. Further, since a line for the Rambus signal, the line requiring preset impedance precision, can be linearly disposed on the surface layer of the board, the impedance on the mother board can be easily controlled.

Next, still another embodiment of this invention is explained with reference to FIGS. 4 and 5.

In the above embodiments, the structure in which a plurality (two in the above embodiments) of SO-RIMMs are arranged on the same surface (one-side surface) of the mother board is explained. In the present

embodiment, the structure in which one SO-RIMM among three SO-RIMMs is arranged on a different surface (the other surface) is shown. In FIGS. 4 and 5, portions which are the same as those of FIG. 2 are denoted by the same reference numerals and the explanation therefor is omitted.

In the construction of the memory device of the present embodiment shown in FIGS. 4 and 5, a first (first-stage) SO-RIMM 13A and a second (second-stage) SO-RIMM 13B are arranged in the same position and different surfaces to face each other with a mother board 40 disposed between the different surfaces. In other words, SO-RIMM sockets 12A, 12B are provided on both sides of the mother board 40. Further, an SO-RIMM socket 12C on which a third (third-stage) SO-RIMM 13C is mounted is arranged in a back-to-back relation with respect to the SO-RIMM socket 12A. In this case, a pattern wiring 18 is wired by use of a through hole between the SO-RIMM socket 12A on which the first (first-stage) SO-RIMM 13A is mounted and the SO-RIMM socket 12B on which the second (second-stage) SO-RIMM 13B is mounted. Further, a pattern wiring 20 is wired between the SO-RIMM socket 12B on which the second (second-stage) SO-RIMM 13B is mounted and the SO-RIMM socket 12C on which the third (third-stage) SO-RIMM 13C is mounted by use of the through hole and the surface layer patterns on which the sockets are

disposed. In addition, a pattern wiring 21 is wired, on the mounting surface of the terminal resistor module (RM) 14, between the SO-RIMM socket 12C on which the third (third-stage) SO-RIMM 13C is mounted and the terminal resistor module (RM) 14.

In this example, all of the three sockets are formed of SO-RIMMs. However, one socket among the three sockets may be mounted on the mother board not as an SO-RIMM socket but as a CSP (Chip Size Package).

Further, a Rambus signal path extending from the memory controller (MEM-CONT) 11 to the terminal resistor module (RM) 14 via the SO-RIMM socket 12B, SO-RIMM socket 12A and SO-RIMM socket 12C can be formed.

Further, in a memory device having two SO-RIMM sockets mounted thereon, a Rambus signal path extending from the memory controller (MEM-CONT) 11 to the terminal resistor module (RM) 14 via the SO-RIMM socket 12A and SO-RIMM socket 12B may be formed.

In either case, the pattern wiring through which the Rambus signal is transmitted is wired so as not to pass through an area in which the SO-RIMM attached to the SO-RIMM socket is mounted. Therefore, an influence on the impedance (28 ohms±10%) by the metal cover of the SO-RIMM can be prevented.

Therefore, a multi-layered circuit board such as a four-layered or six-layered circuit board which is

relatively inexpensive can be used as a mother board and the cost of the whole device is lowered.

Further, according to the mounting structure of the above embodiment, the pattern wirings 17, 18, 20 and 21 for the Rambus signal are provided on the surface layer of the mother board. Therefore, in comparison with a case wherein the Rambus signal line is wired in the internal layer, it becomes easier to attain preset impedance precision and make the pattern design.

In the above embodiments, a memory construction having two SO-RIMMs mounted on the same surface of the mother board is explained as an example. However, this invention is not limited to this memory construction and this invention can also be applied to a memory construction having three or more high-speed memory modules mounted on the same surface of the mother board.

As described above, according to this invention, when a high-speed memory device constructed by connecting a plurality of flat high-speed memory modules, the modules can be cascade-connected between the high-speed memory modules with the impedance of signals in connected lines thereof kept constant by use of an inexpensive multi-layered circuit board structure. Each of the flat high-speed memory modules includes a connector having input side and output side

terminals arranged on one side, the terminals being set for dealing with a high-speed signal of plural-bit width whose impedance is controlled and which is transmitted from a main controller to a terminal resistor is realized thereof.

Further, according to this invention, when a high-speed memory device constructed by connecting a plurality of flat high-speed memory modules each including a connector having input side and output side terminals arranged on one side thereof, for dealing with a high-speed signal of plural-bit width whose impedance is controlled and which is transmitted from a memory controller to a terminal resistor is realized, the surface pattern of a multi-layered circuit board is used and high-speed memory modules can be cascade-connected between the high-speed memory modules with the impedance thereof kept constant. As a result, a stable high-speed memory operation can be attained by use of an inexpensive multi-layered circuit board structure.

Further, according to this invention, when a high-speed memory device is realized by use of a plurality of SO-RIMMs, an inexpensive mother board which has a less number of layers and is advantageous in cost can be used. A Rambus signal requiring determined preset impedance precision is transmitted on the surface layer of the mother board. As a result,

even when the SO-RIMM is mounted, no influence will be given to the Rambus signal pattern on the mother board. Further, the SO-RIMM can be stably operated by use of a mother board of inexpensive layer structure.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. A memory device comprising:

a plurality of storage means for storing information;

means for controlling said storage means;

means, having a resistance, for terminating an electric signal; and

a pattern wiring for electrically connecting said plurality of storage means, said controlling means and said terminating means;

wherein said plurality of storage means, said controlling means and said terminating means are arranged on a board, and said pattern wiring being located in a preset position on the board other than a position in which said storage means is located.

2. The memory device according to claim 1, wherein said pattern wiring is located on an insulating portion of the board surface.

3. The memory device according to claim 2, wherein said pattern wiring is arranged on a surface layer of the board for transmitting the electric signal, and the board being composed of multiple layers.

4. The memory device according to claim 3, wherein the electric signal is a signal transmitted from said controlling means to said terminating means, and an impedance of the electric signal having a preset

value.

5. The memory device according to claim 4, further comprising means for generating a clock signal, and supplying the clock signal to said storage means connected to said terminating means.

6. The memory device according to claim 5, wherein said plurality of storage means at least including:

first storage means for receiving an output signal from said controlling means, and said first storage means being arranged on a front surface of the board, and an input terminal of said first storage means facing an output terminal of said controlling means;

second storage means for receiving an output signal from said first storage means, and said second storage means being arranged on a reverse surface of the board; and

third storage means for receiving an output signal from said second storage means, and an output terminal of said third storage means facing an input terminal of said terminating means;

wherein said pattern wiring is at least arranged between said controlling means and said first storage means, between said storage means, and between said third storage means and said terminating means.

7. The memory device according to claim 5, wherein said plurality of storage means at least

including:

first storage means for receiving an output signal from said controlling means, and said first storage means being arranged to face an output terminal of said controlling means; and

second storage means for receiving an output signal from said first storage means, said second storage means being arranged to face an output terminal of said first storage means, and an output terminal of said second storage means being arranged to face an input terminal of said terminating means;

wherein said pattern wiring is at least arranged between said controlling means and said first storage means, between said storage means, and between said second storage means and said terminating means.

8. The memory device according to claim 7, wherein an input terminal of said first storage means is arranged to face the output terminal of said second storage means;

the output terminal of said first storage means is arranged to face an input terminal of said second storage means; and

wherein said pattern wiring is arranged between terminals of said first and second storage means.

9. The memory device according to claim 7, wherein only the output terminal of said first storage means and an input terminal of said second storage

means among the terminals of said first and second storage means are arranged to face each other, and said pattern wiring being arranged between said first and second storage means.

10. The memory device according to claim 7, wherein at least two of said plurality of storage means are individually provided in each of the front and reverse surfaces of the board, and said pattern wiring being connected between said storage means.

11. A socket mounting structure of a memory device comprising:

a plurality of storage means for storing information;

means for controlling said storage means;

means, having a resistance, for terminating an electric signal; and

a pattern wiring for electrically connecting said plurality of storage means, said controlling means and said terminating means;

wherein said plurality of storage means, said controlling means and said terminating means are mounted on a board, and said pattern wiring being located in a preset position on the board other than a position in which said storage means is located.

12. The socket mounting structure of the memory device according to claim 11, wherein said pattern wiring is located on an insulating portion of the board

surface between said controlling means and said terminating means.

13. The socket mounting structure of the memory device according to claim 12, wherein the electric signal is transmitted via a surface layer pattern of the board, and the board being composed of multiple layers.

14. The socket mounting structure of the memory device according to claim 13, wherein the electric signal is a signal transmitted from said controlling means to said terminating means, and an impedance of the electric signal having a preset value.

15. The socket mounting structure of the memory device according to claim 14, further comprising means for generating a clock signal, and supplying the clock signal to said storage means connected to said terminating means.

16. A mounting method of a memory device comprising:

mounting on a board a plurality of storage means for storing information;

mounting on the board a means for controlling said storage means;

mounting on the board a means, having a resistance, for terminating an electric signal; and

mounting on the board a pattern wiring for electrically connecting said plurality of storage

means, said controlling means and said terminating means;

wherein said pattern wiring is located in a preset position on the board other than a position in which said storage means is located.

17. The mounting method of the memory device according to claim 16, wherein said pattern wiring is mounted on an insulating portion of the board surface between said controlling means and said terminating means.

18. The mounting method of the memory device according to claim 17, wherein said pattern wiring is arranged on a surface layer of the board for transmitting the electric signal, and the board being composed of multiple layers.

19. The mounting method of the memory device according to claim 18, wherein the electric signal is transmitted from said controlling means to said terminating means, and an impedance of the electric signal being adjusted to have a preset value.

20. The mounting method of the memory device according to claim 19, further comprises mounting means for generating a clock signal, and supplying the clock signal to said storage means connected to said terminating means.

ABSTRACT OF THE DISCLOSURE

In this invention, SO-RIMM sockets are arranged on a mother board so that an output side terminal of a connector provided on a preceding-stage SO-RIMM and an input side terminal of a connector provided on a succeeding-stage SO-RIMM will be set to face each other at a close distance. Therefore, in a high-speed memory device constructed by connecting a plurality of flat high-speed memory modules each including a connector on one side of which input side and output side terminals for dealing with a high-speed signal of plural-bit width whose impedance is controlled and which is transmitted from a memory controller to a terminal resistor are arranged, a high-speed memory device in which high-speed memory modules can be cascade-connected and which can maintain the impedance of a memory bus signal in a constant value by use of an inexpensive multi-layered circuit board structure, a socket mounting structure of the high-speed memory device and a mounting method of the high-speed memory device can be provided.

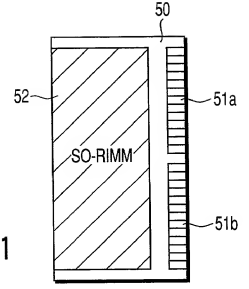
50
52
51a
SO-RIMM
51b

FIG. 1

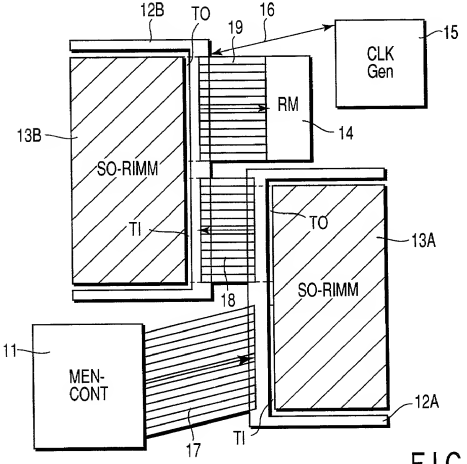
12B
TO
19
16
CLK
Gen
15
RM
14
13B
SO-RIMM
TI
TO
13A
18
SO-RIMM
11
MEN-
CONT
12A
17
TI

FIG. 2

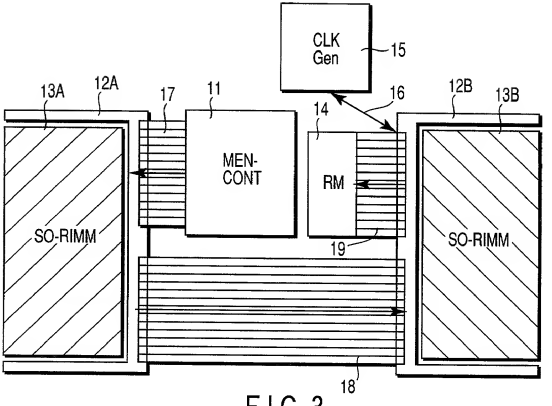
CLK
Gen
15
13A
12A
17
11
14
16
12B
13B
MEN-
CONT
RM
SO-RIMM
SO-RIMM
19
18

FIG. 3

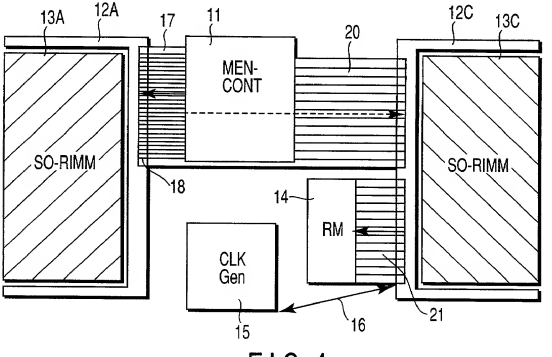
13A
12A
17
11
20
12C
13C
MEN-
CONT
SO-RIMM
SO-RIMM
18
14
RM
CLK
Gen
15
16
21

FIG. 4

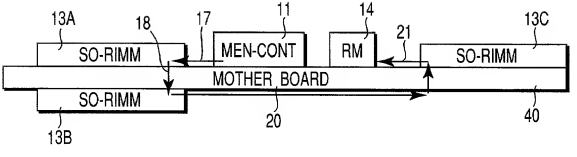
13A
18
17
11
14
21
13C
SO-RIMM
MEN-CONT
RM
SO-RIMM
MOTHER BOARD
SO-RIMM
13B
20
40

FIG. 5

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I declare:
that verily believe myself to be the original, first and sole (if only one individual inventor is listed below) or an original, first and joint inventor (if more than one individual inventor is listed below) of the invention in

HIGH-SPEED MEMORY DEVICE, SOCKET MOUNTING STRUCTURE FOR MOUNTING A HIGH-SPEED MEMORY DEVICE AND MOUNTING METHOD OF MOUNTING HIGH-SPEED MEMORY DEVICE

the specification of which is attached hereto unless the following box is checked.

☐ was filed on _____ as United States Application or PCT International Application No. _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information of which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365 (b) of any foreign application(s) for patent or inventor's certificate, or 35 U.S.C. 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Country	Category	Application No.	Filing Date	Priority Claim
Japan	Patent	11-278225	September 30, 1999	Yes

And I hereby appoint Stephen A. Bent (Reg. No. 29,768), David A. Blumenthal (Reg. No. 26,257), Beth A. Burrous (Reg. No. 35,087), Alan I. Cantor (Reg. No. 28,163), William T. Ellis (Reg. No. 26,874), John J. Feldhaus (Reg. No. 28,822), Patricia D. Granados (Reg. No. 33,683), John P. Isacson (Reg. No. 33,715), Michael D. Kaminski (Reg. No. 32,904), Lyle K. Kimms (Reg. No. 34,079), Kenneth E. Krosin (Reg. No. 25,735), Johnny A. Kumar (Reg. No. 34,649), Glenn Law (Reg. No. 34,371), Peter G. Mack (Reg. No. 26,001), Brian J. McNamara (Reg. No. 32,789), Sybil Meloy (Reg. No. 22,749), Richard C. Peet (Reg. No. 35,792), George E. Quillin (Reg. No. 32,792), Colin G. Sandercock (Reg. No. 31,298), Bernhard D. Saxe (Reg. No. 28,665), Charles F. Schill (Reg. No. 27590), Richard L. Schwaab (Reg. No. 25,479), Arthur Schwartz (Reg. No. 22,115) and Harold C. Wegner (Reg. No. 25,258), each of whose address is 3000 K Street, N.W., Suite 500, Washington, D. C. 20007-5109, or any one of them, my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent & Trademark Office connected therewith, and request that correspondence be directed to Foley & Lardner, 3000 K Street, N.W., Suite 500, Washington, D. C. 20007-5109.

I declare further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

DECLARATION FOR PATENT APPLICATION

I declare further that my post office address is at c/o Intellectual Property Division, KABUSHIKI KAISHA TOSHIBA, 1-1 Shibaura 1-chome, Minato-ku, Tokyo 105-8001, Japan; and that my citizenship and residence are as stated below next to my name:

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